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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Date: February 14, 2002

In re Application of: R. T. Bailis et al.

Serial Number: 10/015,921

Filed: December 10, 2001

For: Method and System for Use of a Field Programmable Gate Array (FPGA) Cell for Controlling Access to On-Chip Functions of a System on a Chip (SOC) Integrated Circuit Chip

Art Unit: 2811

Examiner:

TRANSMITTAL OF CORRECTED APPLICATION PAPERS

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

In response to the "Notice to File Corrected Application Papers" mailed January 11, 2002, attached are 2 sheets of Formal Drawings.

Respectfully submitted,

By Joscelyn G. Cockburn

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